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10/609,042	06/27/2003	Louis A. Lippincott	42P17010	8378

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EXAMINER	
MONESTIME, MACKLY	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,042	LIPPINCOTT, LOUIS A.	
	Examiner	Art Unit	
	Mackly Monestime	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 8-15, 18-1 are rejected under 35 U.S.C. 102(b) as being anticipated by Gannett (US Patent No. 5,790,130).

4. As per claims 1, 12, 20, 24, Gannett disclosed the invention as claimed including an image signal processor comprising: a local memory to store data (Fig. 3, Item No. 155); and a memory command handler including a plurality of memory address generators (Fig. 3A, Items No. 170, 172 and 174), each memory address generator to generate a memory address to the local memory and to interpret a command to be performed on the data of the local memory located at the memory address to aid in image processing tasks (col. 8, lines 21-23; col. 11, lines 13-20).

5. As per claims 2, 13, 21, Gannett disclosed a shared memory coupled to the plurality of the memory address generators, the shared memory storing data to be sent to the local memory and commands to be performed by the memory address generators (col. 9, lines 30-34; col. 69, lines 42-52).

6. As per claims 3-4, 14, 22, Gannett disclosed the shared memory comprises a plurality of cluster communication registers a cluster communication register interface to couple the plurality of cluster communication registers to the plurality of memory address generator (col. 16, lines 22-23).

7. As per claims 5, 15, 23, Gannett disclosed that the plurality of clusters communication registers include data cluster communication registers to store data and command cluster communication registers to store command (col. 42, lines 60-67; col. 43. lines 1-2).

8. As per claims 8, 25 Gannett did not explicitly disclose an arbiter to arbitrate to the local memory by the memory address generator. However, Gannett did teach that the texture interrupt managing manages the texture memory, controls the socketed communication with each of the hardware drivers and, when hardware device interrupts occur, implements routines (which, in turn, call device dependent routines) to determine which blocks of texture data are needed by the hardware devices and which blocks of texture data within the local memories of the hardware devices should be overwritten (col. 12, lines 46-53). Therefore, Gannet inherently disclosed an arbiter.

9. As per claims 9-10, 18-19, 26-27 Gannett disclosed that the plurality of cluster registers are at least 16 bit registers and 16 bit data path coupled to the registers (col. 25, lines 40-44; col. 24, lines 40-45).

10. As per claim 11, Gannett disclosed a static random access memory (SRAM) (col. 23, lines 19-21).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 6-7, 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gannett (US Patent No. 5,790,130).

13. As per claims 6, 16 Gannett did not explicitly disclose a pair of cluster communication registers is assigned to each memory address generator. However, Gannett did show the use of a textel port registers used by the texture interrupt managing and allowing simultaneous writing and reading of data (col. 45, lines 26-44; col. 52, lines 12-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to assign a pair of registers to each memory address generator because doing so would provide simultaneous access to the registers in an interleave fashion.

14. As per claim 7, Gannett disclosed each pair of cluster communication registers includes a data cluster communication register and a command cluster communication register (col. 42, lines 60-67; col. 43. lines 1-2).

15. As per claim 17, Gannett did not disclose an arbiter to arbitrate to the local memory by the memory address generator. However, Gannett did teach that the texture interrupt managing manages the texture memory, controls the socketed communication with each of the hardware drivers and, when hardware device interrupts occur,

implements routines (which, in turn, call device dependent routines) to determine which blocks of texture data are needed by the hardware devices and which blocks of texture data within the local memories of the hardware devices should be overwritten (col. 12, lines 46-53). Therefore, Gannet inherently disclosed an arbiter.

16. Claims 28-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gannett (US Patent No. 5,790,130) in view of Burton (US Pub. No 2004/0236877).

17. As per claims 28-29, Gannett substantially disclosed the invention as claimed, including an image processor system comprising: a processor coupled to an image processor (Fig. 4, Items No. 19, 10); and a plurality of image processors coupled to one another (Fig. 3); each image processor including: a local memory to store data (Fig. 3, Item No. 155); and a memory command handler including a plurality of memory address generators (Fig. 3A, Items No. 170, 172 and 174), each memory address generator to generate a memory address to the local memory and to interpret a command to be performed on the data of the local memory located at the memory address to aid in image processing tasks (col. 8, lines 21-23; col. 11, lines 13-20).

18. Gannett did not disclose a double data rate synchronous dynamic random access memory. However, Burton disclosed the use of a double data rate synchronous dynamic random access memory (page 3, paragraph 0030; page 6, paragraph 0051). Moreover, it is well known in the memory art that DDR-SDRAM includes clock rates of from 200-400MHz; as is also well known DDR-SDRAM captures write data by using the timing signal and the inversion clock signal, and arranges the write data in parallel within; and also supports writing and reading of data on both rising and falling edges of

the write and read clock signals. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the present invention was made to have included the DDRSDRAM taught by Burton into the teachings of Gannett because doing so would provide high-rate data transfer, thereby enhance the overall processing of the system.

19. As per claims 30-31, Gannett disclosed the shared memory comprises a plurality of cluster communication registers a cluster communication register interface to couple the plurality of cluster communication registers to the plurality of memory address generator (col. 16, lines 22-23).

20. As per claim 32, Gannett disclosed that the plurality of clusters communication registers include data cluster communication registers to store data and command cluster communication registers to store command (col. 42, lines 60-67; col. 43. lines 1-2).

21. As per claims 3334, Gannett did not explicitly disclose a pair of cluster communication registers is assigned to each memory address generator. However, Gannett did show the use of a textel port registers used by the texture interrupt managing and allowing simultaneous writing and reading of data (col. 45, lines 26-44; col. 52, lines 12-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to assign a pair of registers to each memory address generator because doing so would provide simultaneous access to the registers in an interleave fashion.

22. As per claim 35, Gannett did not explicitly disclose an arbiter to arbitrate to the local memory by the memory address generator. However, Gannett did teach that the texture interrupt managing manages the texture memory, controls the socketed communication with each of the hardware drivers and, when hardware device interrupts occur, implements routines (which, in turn, call device dependent routines) to determine which blocks of texture data are needed by the hardware devices and which blocks of texture data within the local memories of the hardware devices should be overwritten (col. 12, lines 46-53). Therefore, Gannet inherently disclosed an arbiter.

23. As per claims 36-37 Gannett disclosed that the plurality of cluster registers are at least 16 bit registers and 16 bit data path coupled to the registers (col. 25, lines 40-44; col. 24, lines 40-45).

24. As per claim 38, Gannett disclosed a static random access memory (SRAM) (col. 23, lines 19-21).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mackly Monestime whose telephone number is (571) 272-7786. The examiner can normally be reached on Monday to Thursday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bella Matthew, can be reached on (571) 272-7778.

Any response to this action should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,

Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Mackly Monestime

Patent Examiner

March 15, 2005